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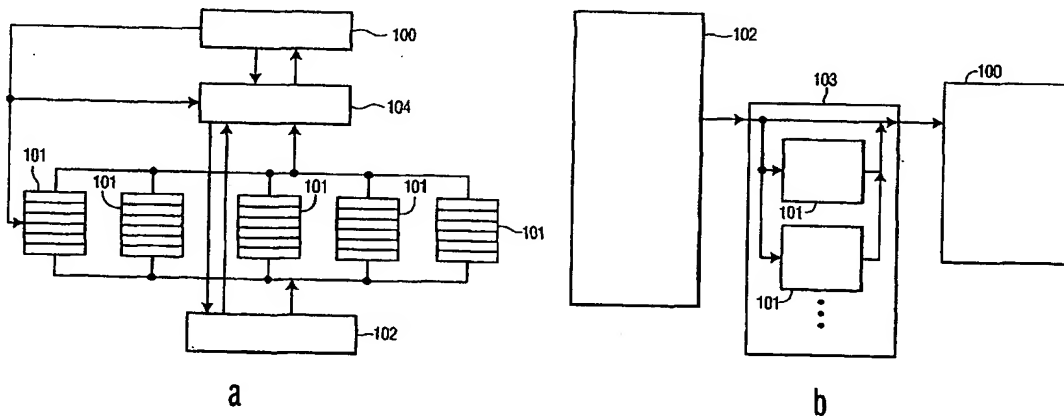
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[Continued on next page]

(54) Title: USING A CACHE MISS PATTERN TO ADDRESS A STRIDE PREDICTION TABLE



(57) Abstract: Data prefetching is used to reduce an average latency of memory references for retrieval of data therefrom. The prefetching process is typically based on anticipation of future processor data references. In example embodiment, there is a method of data retrieval that comprises providing a first memory circuit (610), a stride prediction (611) table (SPT) and a cache memory circuit (612). Instructions for accessing data (613) within the first memory are executed. A cache miss (614) is detected. Only when a cache miss is detected is the SPT accessed and updated (615). A feature of this embodiment includes using a stream buffer as the cache memory circuit. Another feature includes using random access cache memory as the cache memory circuit.

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